A Review on Field Programmable Gate Arrays Control Based Photovoltaic Energy Management

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Abstract -- This Paper is about research on the Field Programmable Gate Arrays Control Based PV Systems. Sun oriented Photovoltaic (PV) vitality is turning into an undeniably vital piece of the world's sustainable power source. This paper centers around the sun based power framework and the present advances to enhance the proficiency of the Solar PV framework. The utilization of Renewable is expanding quickly because of less accessibility of ordinary vitality hotspots for age of power. The sun oriented vitality is effectively accessible with no cost and establishment is likewise simple and Solar PV System is presently turned out to be best innovation to create power from sun based vitality so the fundamental piece of the paper is FPGA based investigation which is performed in France. To comprehend the analysis the basic piece of the entire framework are depicted quickly. The control calculation and coding for coordination with the PV cell is proposed by methods for the VHDL code and actualized utilizing Xilinx Spartan-3 from Digilent (NEXYS-2) FPGA board. This has all been done, and the entire undertaking works including the control of chopper and showing the estimations of the streams and voltages. The created equipment has the benefits of simple programming in VHDL with high precision even with low determination ADC which are used in microcontroller and dSPACE.

Indexed Terms -- Photovoltaic, XILINX, FPGA, DC/DC Buck converter

I. INTRODUCTION

In the advanced time the request of Electricity is increment so for satisfaction of the required power at crest hours we require sustainable power sources in light of the fact that regular vitality sources are diminishing step by step and close to the end. Sustainable power sources, for example, sun based vitality, wind vitality are obtaining more essentialness. The photovoltaic (PV) framework for changing over sun based vitality into power is by and large expensive and is a fundamental method for power age just on the off chance that it can create the greatest conceivable yield for every climate condition. The PV exhibit has an exceedingly non straight current-voltage trademark shifting with the irradiance and temperature that significantly influences the cluster control yield. The most extreme power point following MPPT control of the PV framework is accordingly basic for the achievement of a PV framework [1]-[3].

A field-programmable entryway exhibit (FPGA) is an integrated circuit intended to be arranged by the client or fashioner subsequent to assembling thus "field-programmable". The FPGA arrangement is for the most part determined utilizing an equipment portrayal dialect (HDL). FPGAs contain programmable rationale parts called "rationale pieces", and a chain of command of reconfigurable interconnects that enable the squares to be "wired together"— fairly like many (alterable) rationale entryways that can be between wired in (many) distinctive designs. To characterize the conduct of the FPGA, the client gives an equipment portrayal dialect (HDL) or a schematic outline. The HDL frame is more suited to work with extensive structures since it's conceivable to simply indicate them numerically as opposed to drawing each piece by hand. Uses of FPGAs incorporate computerized flag handling, programming characterized radio, aviation and safeguard frameworks, ASIC prototyping, medicinal imaging, PC vision, discourse acknowledgment, cryptography, bioinformatics, PC equipment copying, radio space science, metal discovery and a developing scope of different zones.

XILINX FPGA and configuration devices empower to create model rationale outlines in a brief period. It is conceivable to make, execute, and confirm another plan. A configuration program put away in inner static memory cells of the XILINX FPGA is composed by VHDL programming dialect that has been outlined and improved for portraying the conduct of

computerized frameworks. VHDL has numerous highlights fitting for portraying the conduct of electronic segments extending from straightforward rationale entryways to finish microchips and custom chips. Highlights of VHDL permit electrical parts of circuit conduct, (for example, rise and fall times of signs, delays through doors, and practical activity) to be unequivocally depicted. The utilization of FPGAs rather than different models was chiefly in light of four factors: the increasing speed of the plan or parts of it, the adaptability of equipment reconfiguration, the diminishment of expenses, and the vitality utilization [3].

A few advanced circuits have been proposed and utilized for PV module which go from DSP [1], dSPACE, microcontroller yet Field Programmable Gate Array (FPGA) [2], [3] based frameworks could give various run-time preferences over the successive machines, for example, a microcontroller and dSPACE. FPGAs are progressively utilized as a part of ordinary elite figuring applications where computational portions (Fast Fourier change, convolution and so on) are performedon FPGA rather than on processor. FPGA usage ofthese parts offers request of size execution upgrades over microchips. Different advantages are as far as power utilized: a FPGA usage of FFT or SCEECS 2012 convolution is relied upon to devour lesser power than a chip. Low-control use is because of the lower "clock rate" and truly no squandered cycles for direction bring/translate as in CPUs. Additionally, with simultaneous activity, it is executed consistently and all the while which is quicker than DSP. In this manner the FPGA has been connected for fast changing circuit to decrease hardware measuring [3] particularly in the usage. This paper is sorted out as takes after: Section II demonstrates the proposed framework design. In area III Design of electronic card is talked about and programming of XILINX card (FPGA) utilizing VHDL .The DC/DC converter and DC/AC inverter arrangement is examined in segment IV. Trial comes about are appeared in segment V. At last conclusions are displayed in area VI.

II. THE PROPOSED FPGA SYSTEM

The easiest comparable circuit of a sun oriented cell is a present source in parallel with a diode. The yield of the present source is straightforwardly corresponding to the light falling on the cell. The diode decides the attributes of the cell.

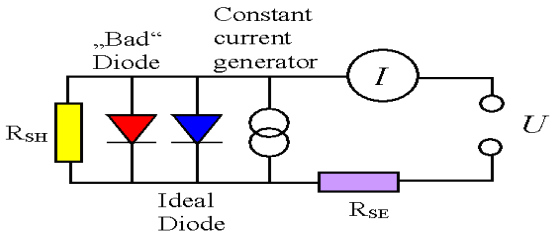

Fig. 1: - The circuit model diagram of Solar cell

The system consists of a solar array, buck converter, XILINX (FPGA) Board, Battery, inverter. The type of solar cell used is PW1650 from Photo watt (BOURGOIN-JALLIEU - France). Its electrical characteristics can be up to 200W @ 00 C. The maximum electrical characteristics obtained during our unrepeatable tests (clouds) are given in Table. 1.

ELECTRICAL CHARACTERISTICS OF PV MODULE

Rated Power (Pmax)	67W
Voltage at Pmax (Vmp)	21.07V
Current at Pmax (Imp)	3.2A
Open circuit voltage (Voc)	24.7V
Short circuit current (Isc)	5A

Table 1

III. DC/DC CONVERTER CONFIGURATION

The dc-dc converter creates a hacked yield voltage and in this manner controls the normal dc voltage connection between its info and yield going for constantly coordinating the normal for the PV framework to the equal impedance displayed by the dc side of inverter. The unfaltering state voltage and current relations of the Buck converter working in ceaseless current mode are given by:

$$V_{out}=V_{in}*D$$

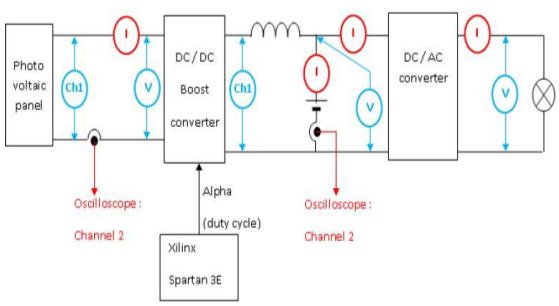

Fig. 2: - Control Design with converter and inverter

DESIGN SPECIFICATION OF BUCK CONVERTER

Input voltage (Vs) Theoretical Experimental	0V-48V 21.07V-38.63V
Input current (Is) Theoretical Experimental	0A-5.5A 0A-3.2A
Output Voltage (Vo) Theoretical Experimental	12V 11.57V-14.42V
Output current (Io)	0A-4.35A
Maximum Power output (Pmax)	52.9W
Switching frequency (f)	16.86kHz
Duty cycle (D)	0.32-0.82

Table 2

IV. THE FPGA LAYOUT

The whole digital design has been implemented in VHDL, using Xilinx software, to be able to use the Spartan3 FPGA. First, it was necessary to study the Xilinx development tool.

V. VOLTAGE AND CURRENT SENSING

For current measurement, the hardware topology uses current transducers in the form of LEM (LA25-NP) implemented on the electronic card which is used to convert the quantity into current entity, then voltage entity for finally converting into digital signal by AD622.

The output of voltage and current signals from PV panel projected onto oscilloscope is shown in Fig. 6 with 40 Watt lamp load. The duty cycle of DC/DC converter is adjusted to be 0.74 while PV output voltage=21.07V and PV output current=3.2A is obtained. The maximum power output from photovoltaic panel for this trial is 67.42 Watt. We caneasily notice here in Fig. 6 that the DC/AC converter doesn't have a strictly constant current: we can see portion of 50 Hz current from the lamp. The current is negative which means that the battery is in charging mode.

VI. THE MPPT

a) Characteristic of a PVarray:

Typically, a PV array comprises of a number of solar cellsconnected in either series or parallel. Its mathematical model may be given as

$$P = n_p I_{ph} V - n_p I_o \left(\exp\left(K_o \left(\frac{V}{n_s} + I_T R_{sT} \right) \right) - 1 \right) V - (V/n_s + I_T R_{sT}) V / R_{shT},$$

where P denotes the output power (W), V denotes the output voltage of the PV array (V), I_{ph} denotes the current of the PV array that is proportional to light intensity (A), $I_T$denotes the output current proportional to temperature (A), I, denotes the array's reverse saturation current (A), R_{ST} and R_{shT} are defined as the equivalent series and parallel resistance (Ω) respectively, n_s is the number of series string in the PV array, $n_p$is the number of parallel string in the PV array and K_0 is a constant.

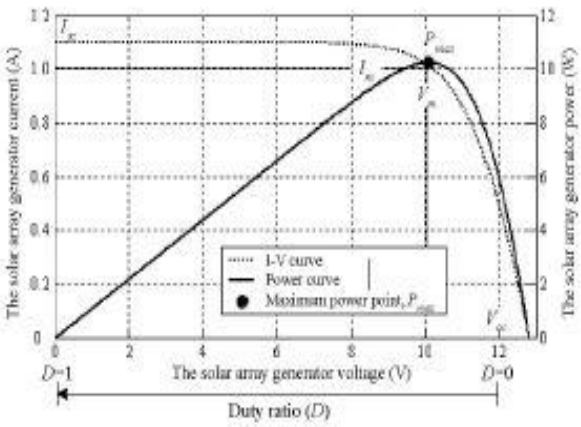

Fig. 1. I-V and Power curve under light intensity and temperature.

Table I
PV array specification (25°C, 100mW/cm²)

Parameters	Definitions
Maximum power, P_{max}	10.0W
Voltage at Maximum power point, V_m	10.0V
Current at Maximum power point, I_m	1.0A

Table II
MPPT Using Modified P&O Method

```
if((P(k) – P(k-1))>0)
   if((V(k) – V(k-1))>0
      D=D-ΔD;
   else D=D+ΔD;
   end
 else
   if((V(k) – V(k-1))>0
      D=D+ΔD;
   else D=D-ΔD;
   end
 end
```

b) Variable step-size P&O algorithm:

The P&O algorithm operates by periodically perturbing the control variable and comparing the instantaneous PV output power after perturbation with that before. In an original MPPT controller using P&O method the adjustment of the operating point is achieved by changing the reference voltage of the controller. However, the adjustment can be made through the duty ratio D. The algorithm is summarized in Table II.

Note that V(k) and P(k) are output voltage and the power of PV which is calculated from V(k)xI(k) at time k, respectively.Besides, D and ΔD respectively denote duty ratio and change of duty ratio. To achieve faster MPPT response and more accurate MPP under dynamic environment, variable perturbation step-size, i.e. ΔD can be employed. In fact, ΔD can be selected as function ofPV power as:

$$\Delta D(k) = \alpha \cdot \beta\left(P(k) - P(k-1)\right),$$

Where α is the constant value to control the movement toward the MPP and the accuracy of convergence for MPPT, β is the sign of step dependent on perturbation direction.

c) Partially Variable step-size INR Algorithm:

The step size for the INC MPPT determines how fast the MPP is tracked. Fast tracking can be achieved with bigger increments, but the system might not run exactly at the MPP but instead oscillate around it; thus, there is a comparatively low efficiency. This situation is inverted when the MPPT is operating with a smaller increment. Therefore, a satisfying tradeoff between the dynamics and oscillations has to be made for the fixed step-size MPPT. The variable step-size iteration [3], [10] can solve the tough design problem. The derivative ofpower to voltage (*dP/dV)*of a PV array was introduced as a suitable parameter for regulating the variable increment for theINC MPPT algorithm in [11]. In this paper, the derivative of power to current (*dP/dI*), as shown in Fig. 1, is employed to determine the variable increment for the proposed INR MPPT algorithm which has a duality relation with the INC MPPT.

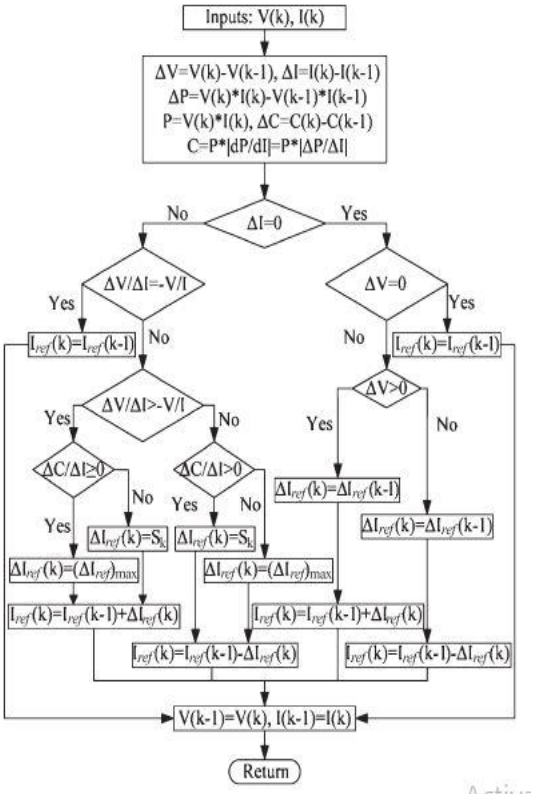

Fig. 5. Flowchart of the partially variable step-size INR MPPT algorithm.

VII. EXPERIMENTAL RESULT

The output of voltage and current signals from PV panel projected onto oscilloscope is shown in Fig. 6 with 40 Watt lamp load. The duty cycle of DC/DC converter is adjusted to be 0.74 while PV output voltage=21.07V and PV output current=3.2A is obtained. The maximum power output from photovoltaic panel for this trial is 67.42 Watt. We can easily notice here in Fig. 6 that the DC/AC converter doesn't have a strictly constant current: we can see portion of 50 Hz current from the lamp. The current is negative which means that the battery is in charging mode.

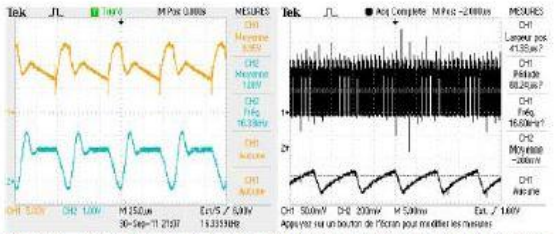

Figure 6. The output voltage and output current respectively from PV at time T1 during the day P=67.42W

The results are performed in Grenoble, France. The proposed setup has been tested at different time during the day (T1, T2) to ensure the testing is done for different environmental operation conditions (with and without clouds). Fig. 6 - 8 show the performance results obtained from the hardware setup for different time during the day, also with different load. Fig. 6 is done for maximum power at 67.42 Watt, output voltage at lamp load=222 volts and duty cycle 0.74 where you can see that current is not exactly constant. With small time difference Fig. 7 has been captured to show the capability of the control with FPGA and then the load energy is coming both from PV and battery. In Fig. 7 (also at T2) it can be notice that Ibattery> 0 (battery is in generator mode) (3.3W).

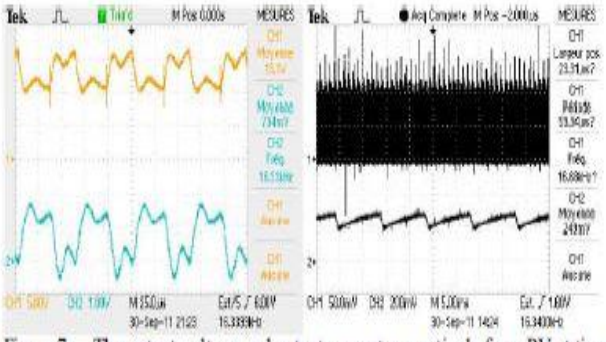

Figure 7. The output voltage and output current respectively from PV at time T2 during the day P=44.05W

At t=T2 the extracted power from PV is 44.05 Watt and PV output voltage=25.17V, PV output current=1.75 Ampere respectively at duty cycle 0.56. At t=T2, the load (same lamp), as in the time T1 as the same consumption power (34W). Simultaneously we can notice in Fig. 7 that the DC/AC converter doesn't have a strictly constant current it is due to the fact that solar insolation is fluctuating very fast in the region where the experiments are performed. Fig. 8 shows the PV voltage and current waveforms in "same as possible" condition than T3, but without lamp load of

wattage capacity 40W (34W real). The PV output voltage=27.6V, PV output current=1.3A and maximum power 35.1W. Fig. 8 shows the output voltage from DC/DC converter when there is no load connected and current output from the battery. The whole solar energy is going through the battery which is in charging mode.

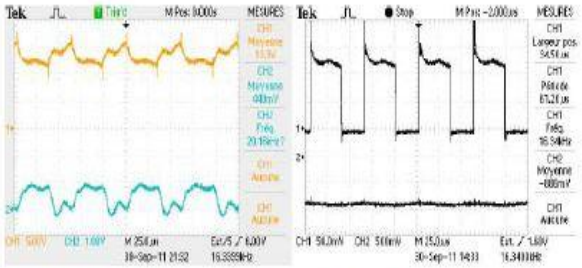

Figure 8. The output voltage and output current respectively from PV at time T3 during the day P=35.92W

VIII. CONCLUSION

The objective of the venture was to control the chopper in orderto have the capacity to charge a battery and sustain a heap with vitality from that battery and additionally the sun based board, and show all the noteworthy signs. In this way it was important to influence an equipment to card and a product usage on a FPGA. This has all been done, and the entire venture works, including the control of the chopper and showing the estimations of the streams and voltages. It would have been exceptional to control the chopper in shut circle rather than the open circle framework that we utilized. Along these lines it is conceivable to ensure that the solar panels works in its ideal power point, by utilizing a MPPT.

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